REMARKS/ARGUMENTS

This Amendment is in response to the Final Office Action dated January 6, 2004. Claims 1-11 are pending in the present application. Claims 1-11 have been rejected. Claims 1, 4, 6, 8, and 10 have been amended to further define the scope and novelty of the present invention, as well as to correct typographical and grammatical errors. Support for the amendments to the claims is found throughout the specification, and in particular, in Figure 3 and on page 6, line 13, to page 7, line 5. Applicants respectfully submit that no new matter has been presented. Accordingly, claims 1-11 are pending. For the reasons set forth more fully below, Applicants respectfully submit that the claims as presented are allowable. Consequently, reconsideration, allowance, and passage to issue are respectfully requested.

In the event, however, that the Examiner is not persuaded by Applicants' amendments and arguments, Applicants respectfully request that the Examiner enter the amendments and arguments to clarify issues upon appeal.

Rejection Under 35 U.S.C. §102

The Examiner has stated:

> **Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Lien et al. (US 6,211,697 B1).**
>
> **Regarding claims 1-7, Lien et al. discloses, in figure 11, an ASIC comprising:**
>
> **a standard cell (HA) including a plurality of logic functions (col. 4, lines 63+); a plurality of input output pins (col. 5, line 47); and at least one FPGA interconnect (see 48-56 in fig. 2) coupled to the plurality of I/O pins and the plurality of logic functions, wherein the at least one FPGA interconnect can be configured to select one of the plurality of logic functions (via lines G/2) utilizing field programming techniques (see IGs 26-34 and 58-100 in fig. 2); and wherein the one logic function is coupled to an internal bus (see 48-56 in fig. 2) via the at least one configured FPGA interconnect.**
>
> **Regarding claims 8 and 9, utilizing at least one FPGA interconnect to correct wiring error which is a reversed bit order wiring error, when the ASIC is utilized on a printed circuit board, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus**

from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Regarding claims 10 and 11, Lien et al. discloses, in figure 9B, an ASIC comprising:

a plurality of I/O pins (col. 5, line 47);

a plurality of first logic functions (logic functions in HA 210) provided as part of a standard cell (HA 210-216);

a first FPGA interconnect (FPGA 218) coupled between the plurality of I/O pins and the plurality of first logic function, wherein the first FPGA interconnect can be configured to select at least one of the plurality of first logic functions (300 in Fig. 15 in combination with internal bus of FPGA 218, see fig. 2);

a bus (see 48-56 in Fig. 2; and 300 in Fig. 15) coupled to the plurality of first logic functions;

a second FPGA interconnect (FPGA 222) coupled between the bus and the plurality of first logic functions, wherein the second FPGA interconnect is configured to connect to one of the plurality of first logic functions to the bus (see col. 11, lines 23+); and

a plurality of second logic functions (HA 212) coupled to the bus. ...

Applicant argues, on page 7, that the FPGA interconnect can be configured to select one of the plurality of logic functions .... However, Figure 3 of Lien shows transistors and memory cells (e.g. 302, M88 in Fig. 15) that are selectively configured (at the time of programming) so that the FPGA interconnect (G in Fig. 15) can be configured to select one of the plurality of logic functions of the standard cell (HA 250 or 252 in Fig. 15).

As to claims 8 and 9, applicants argues, on page 7, that "there is no teaching suggestion that the FPGA can be utilized to correct a wiring error". However, ...when the user finds a wiring error ... the user can always modify the program to use the other wire. ...

Applicants respectfully traverse the Examiner's rejections. For the Examiner's convenience, amended independent claim 1 is reproduced in its entirety herein below.

Claim 1

1. (currently amended) An application specific integrated circuit (ASIC) comprising:

a standard cell, the standard cell including a plurality of logic functions; and

at least one FPGA interconnect coupled to the plurality of functions, wherein the at least one FPGA interconnect can be configured to select one of the plurality of logic functions, wherein the at least one FPGA interconnect can be utilized to correct a wiring error on a printed circuit board by reconfiguring connections through the at least one FPGA interconnect.

The present invention provides an application specific integrated circuit (ASIC) is disclosed. The ASIC comprises a standard cell, the standard cell including a plurality of logic

functions. The ASIC further includes at least one FPGA interconnect coupled to at least a portion of the logic functions. The FPGA interconnect can be configured to select a particular logic function of the plurality of logic functions. An ASIC in accordance with the present invention allows "field selection" of functions that are connected to the internal buses and to external I/O. The at least one FPGA interconnect can be utilized to correct a wiring error on a printed circuit board by reconfiguring the connections through the at least one FPGA interconnect. The wiring error can be a reversed bit order wiring error. The functional block connections made with internal buses can be significantly wider and faster than buses brought on chip via external chip I/Os. Further, the ASIC reduces cost because selective bus connections can be made internal to the chip, thus eliminating the need for additional external pins. Finally, the ASIC reduces the cost of the packaged component by allowing the chip to be packaged in a lower pin count package (Summary and page 6, line 13, to page 7, line 5). Lien does not teach or suggest these features, as discussed below.

Lien discloses an integrated circuit (IC) that includes a field-programmable gate array (FPGA) and a hard array (HA). The FPGA is based on a specific underlying logic and routing structure and includes a plurality of transistors and memory cells coupled to the specific underlying logic and routing structure for programming the specific underlying logic and routing structure. The HA is also based on the specific underlying logic and routing structure but it does not include transistors and memory cells coupled to the specific underlying logic and routing structure that are used for programming the specific underlying logic and routing structure (Abstract).

However, Lien does not teach or suggest the FPGA interconnect, wherein the "FPGA interconnect can be utilized **to correct a wiring error on a printed circuit board** by reconfiguring connections **through the at least one FPGA interconnect,**" as recited in amended independent claim 1. Instead, Lien teaches an FPGA that utilizes a plurality of transistors and memory cells to program one or more hard arrays (Abstract). Programming a hard array, which involves information at the outputs of the FPGA, is different from correcting a wiring error on a printed circuit board, because a wiring error involves erroneous information at the input of the FPGA. In fact, such a wiring error would cause an FPGA to malfunction, which would affect its ability to properly program a hard array. Nowhere does Lien specifically teach correcting wiring errors on a printed circuit board. Even if the FPGA of Lien may be reprogrammed to connect the incoming lines of the hard arrays to different bus lines as asserted by the Examiner, Lien does not teach or suggest how this corrects a wiring error on a printed circuit board.

Furthermore, the at least one FPGA interconnect of the present invention can be utilized to correct a wiring error on a printed circuit board "by reconfiguring connections **through the at least one FPGA interconnect,**" as recited in amended independent claim 1. In contrast, the FPGA of Lien connects hard arrays by configuring the plurality of transistors and memory cells, which are **external** to the FPGA (Figure 15 and column 13, lines 35-55). Configuring connections external to the FPGA of Lien is clearly different from reconfiguring connections "**through the at least one FPGA interconnect,**" as recited in amended independent claim 1, because the connections **through** the at least one FPGA interconnect are not external connections but are instead internal connections.

Therefore, Lien does not teach or suggest the present invention as recited in amended independent claim 1, and this claim is allowable over Lien.

Independent claims 4, 6, 8, and 10

Amended independent claims 4, 6, 8, and 10 recite an FPGA interconnect, wherein the "FPGA interconnect can be utilized to correct a wiring error on a printed circuit board by reconfiguring connections through" the FPGA interconnect. As described above, with respect to amended independent claim 1, Lien does not teach or suggest these features. Accordingly, the above-articulated arguments related to amended independent claim 1 applies with equal force to claims 4, 6, 8, and 10. Therefore, claims 4, 6, 8, and 10 are allowable over Lien for at least the same reasons as claim 1.

Remaining dependent claims

Dependent claims 2-3, 5, 7, 9, and 11 depend from amended independent claims 1, 4, 6, 8, and 10, respectively. Accordingly, the above-articulated arguments related to amended independent claims 1, 4, 6, 8, and 10 apply with equal force to claims 2-3, 5, 7, 9, and 11, which are thus allowable over the cited reference for at least the same reasons as claims 1, 4, 6, 8, and 10.

Conclusion

In view of the foregoing, Applicants submit that claims 1-11 are patentable over the cited references. Applicants, therefore, respectfully request reconsideration and allowance of the claims as now presented.

Applicants' attorney believes that this application is in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

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March 3, 2004
Date

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